ABSTRACT OF THE DISCLOSURE

An integrated circuit device includes an embedded memory, a built-in self-test (BIST) circuit, an access time measuring circuit, and a built-in detecting circuit. The BIST circuit is coupled electrically to the memory, and is operable so as to perform consecutive test operations upon addressable memory locations of the memory. The access time measuring circuit is coupled electrically to the memory and the BIST circuit, and is operable so as to generate an access time signal corresponding to access time of one of the memory locations that is currently being tested by the BIST circuit. The detecting circuit is coupled electrically to the measuring circuit, monitors a maximum value of the access time signals generated by the measuring circuit during the consecutive test operations, and outputs a maximum access time signal upon completion of the consecutive test operations.